AMENDMENTS TO THE CLAIMS

1. (Original) A power-on reset circuit for generating a reset signal according to a voltage of a power source, the power-on reset circuit comprising:

an oscillator coupled to the power source for generating an oscillation signal having an oscillation frequency that increases as the voltage of the power source increases;

a frequency detector coupled to the power source and the oscillator for outputting a corresponding first output voltage according to the oscillation frequency of the oscillation signal; and

a reset signal generator for generating the reset signal according to the first output voltage.

2. (Original) The power-on reset circuit according to claim 1, wherein the oscillator is a ring oscillator.

3. (Original) The power-on reset circuit according to claim 2, wherein the ring oscillator comprises a plurality of inverters connected in series to form a ring cascade, and the number of the inverters is an odd number greater than one.

4. (Original) The power-on reset circuit according to claim 1, wherein the oscillator is a voltage-controlled oscillator.

5. (Currently Amended) The power-on reset circuit according to claim 1, wherein the frequency detector comprises:

a current source coupled to the power source;

a first capacitor having a first terminal coupled to the current source, and a second terminal that is grounded;

a second capacitor having a first terminal grounded and a second terminal;

a first switch coupled to ~~a~~ the first terminal of the first capacitor and the second terminal of the second capacitor; and

a second switch ~~connected~~ coupled in parallel to the second capacitor;

wherein the first output voltage is output from the first terminal of the first capacitor.

6. (Original) The power-on reset circuit according to claim 5, wherein the first switch and the second switch are controlled by the oscillation signal, the second switch is OFF when the first switch is ON, and the second switch is ON when the first switch is OFF.

7. (Original) The power-on reset circuit according to claim 5, wherein the magnitude of the first output voltage is inversely proportional to the oscillation frequency of the oscillation signal.

8. (Original) The power-on reset circuit according to claim 5, wherein the current source is a resistor.

9. (Original) The power-on reset circuit according to claim 1, wherein the power-on reset circuit is utilized to reset a digital circuit.

10. (Currently Amended) The power-on reset circuit according to claim 1, wherein the reset signal ~~output circuit~~ generator is a comparator circuit.

11. (Original) The power-on reset circuit according to claim 10, wherein the comparator circuit is coupled to the frequency detector and outputs the corresponding reset signal according to the first output voltage and a second output voltage, wherein the reset signal is enabled when the first output voltage is greater than the second output voltage, and the reset signal is disabled when the first output voltage is smaller than the second output voltage.

12. (Original) The power-on reset circuit according to claim 11, wherein the magnitude of the second output voltage is in fixed proportion to the voltage of the power source.

13. (Original) The power-on reset circuit according to claim 12, further comprising a voltage divider to generate the second output voltage.

14. (Original) The power-on reset circuit according to claim 13, wherein the voltage divider comprises:

a first resistor coupled to the power source; and

a second resistor having a first terminal coupled to the first resistor and a second terminal that is grounded;

wherein the second output voltage is output from the first terminal of the second resistor, and the magnitude of the second output voltage is determined by resistances of the first resistor and the second resistor.

15. (Currently Amended) The power-on reset circuit according to claim 1, wherein the reset signal ~~output circuit~~ generator is an inverter for outputting the reset signal according to the first output voltage.

16. (Currently Amended) A power-on reset method comprising the steps of:

~~receiving~~ applying a voltage of a power source;

providing an ~~corresponding~~ oscillation signal according to the voltage of the power source, wherein the oscillation signal has an oscillation frequency that increases as the voltage of the power source increases;

outputting a ~~corresponding~~ first output voltage according to the oscillation frequency of the oscillation signal; and

comparing the first output voltage to a second output voltage for

~~generating~~ outputting a ~~comparing~~ reset signal~~; and~~

~~outputting a reset signal according to the comparing signal;~~

~~wherein the second output voltage is proportional to the voltage of the power source~~.

17. (Canceled)

18. (Currently Amended) The power-on reset method according to claim 16 wherein the first output voltage is determined by a mathematical function inversely proportional to ~~a~~ the oscillation frequency of the oscillation signal.

19. (New) The power-on reset method according to claim 16 wherein the second output voltage is proportional to the voltage of the power source.

20. (New) A method for generating a power-on reset signal, the method comprising the steps of:

receiving a voltage of a power source;

providing an oscillation signal according to the voltage of the power source, wherein the oscillation signal has an oscillation frequency that changes as the voltage of the power source changes;

outputting a first output voltage according to the oscillation frequency of the oscillation signal; and

detecting the first output voltage to generate the power-on reset signal.

21. (New) The method of claim 20, wherein the first output voltage is determined by a mathematical function inversely proportional to the oscillation frequency of the oscillation signal.

22. (New) The method of claim 20, wherein the step of detecting the first output voltage comprises:

comparing the first output voltage to a threshold voltage to generate the reset signal.